In the Specification

Please amend the specification of this application as follows:

Insert the following paragraph before page 1, line 1:

--This application claims priority under 35 U.S.C. §119(e)(1) from U.S. Provisional Application No. 60/243,933 filed October 27, 2000.--

Rewrite the paragraph at page 2, lines 2 to 14 as follows:

--Direct memory access (DMA) controllers are heavily utilized in the field of digital signal processing (DSP). Such controllers can provide enhanced system performance by off loading the task of real-time data transactions from the central processing unit (CPU). The transfer controller with hub and ports architecture (TCHP) described in U.K. Patent Application No. 9901996.9 filed April 10, 1999 entitled TRANSFER CONTROLLER WITH HUB AND PORTS ARCHITECTURE, having a convention application now U.S. Patent ~~Application Serial~~ No. ~~09/543,870 filed April 6, 2000~~ 6,496,740, provides flexibility and performance above and beyond that of previous DMA implementations through increased parallelism, pipelining, and improved hardware architecture.--

Rewrite the paragraph at page 2, lines 15 to 23 as follows:

--Despite their flexibility and improved system performance, all DMA controllers face a common problem. Because DMAs are fundamentally architected to perform memory transactions, the sharing of any addressable resource with another controller poses a significant challenge to system design. Historically, this has been addressed either by multiple porting of ~~said~~ such addressable resources, or through arbitration schemes, ranging from the very simple to the very complex.--

Rewrite the paragraph at page 3, lines 1 to 8 as follows:

--Arbitration for a single-ported addressable resource ~~to~~ also has its pitfalls. If the number of masters in the system becomes very large, the arbitration scheme will typically become either very complex or very inefficient. Furthermore, with a large number of requesters of a resource, requesters on the lowest of the prioritization levels may often be blocked out for long periods of time trying to gain access to the resource.--

Rewrite the paragraph at page 4, lines 10 to 18 as follows:

--The early direct memory access has evolved into several successive versions of centralized transfer controllers and more recently into the transfer controller with hub and ports architecture. The transfer controller with hub and ports architecture is described in U.K. Patent Application No. 9901996.9 filed April 10, 1999 entitled TRANSFER CONTROLLER WITH HUB AND PORTS ARCHITECTURE, having a convention application now U.S. Patent ~~Application Serial~~ No. ~~09/543,870 filed April 6, 2000~~ 6,496,740.--

Rewrite the paragraph at page 6, lines 7 to 24 as follows:

--The present invention deals with the data transfer connecting various memory port nodes as applied to the transfer controller with hub and ports, which is the subject of U.K. Patent Application Number 9909196.9 filed April 10, 1999, having a convention application now U.S. Patent ~~Application Serial~~ No. ~~09/543,870 filed April 6, 2000~~ 6,496,740. The transfer controller with hub and ports is a significant basic improvement in data transfer techniques in complex digital systems and provides many useful features, one of which is the internal memory port which allows connection of a virtually unlimited number of processor/memory nodes to a centralized transfer controller. The centralized transfer controller must be able to transfer data from node to node

with performance relatively independent of how near or remote a node might be from the transfer controller itself. To clarify the problem solved by the present invention, it is helpful to review the characteristics, architecture, and functional building blocks of the transfer controller with hub and ports.--

Rewrite the paragraph at page 14, lines 4 to 11 as follows:

--As described in U.K. Patent Application No. 9901996.9 filed April 10, 1999 entitled TRANSFER CONTROLLER WITH HUB AND PORTS ARCHITECTURE, having a convention application now U.S. Patent ~~Application Serial~~ No. ~~09/543,870 filed April 6, 2000~~ 6,496,740, the transfer controller with hub and ports includes several facilities that simplify the connection of active ports. There are two main facilities to be discussed, the hub interface unit (HIU) and transfer request (TR) bus.--

Rewrite the paragraph at page 23, lines 3 to 14 as follows:

--This invention enables a new type of HIU called a push HIU. The push HIU is similar to the HIU described in the above mentioned U.K. Patent Application No. 9901996.9 filed April 10, 1999 entitled TRANSFER CONTROLLER WITH HUB AND PORTS ARCHITECTURE, having a convention application now U.S. Patent ~~Application Serial~~ No. ~~09/543,870 filed April 6, 2000~~ 6,496,740. A push HIU functions almost identically to a conventional HIU, processing read and write commands from the transfer controller hub and providing buffering to the peripheral side of the HIU. In a push HIU data may be pushed into the HIU from an active port before a read command is issued to the port.--